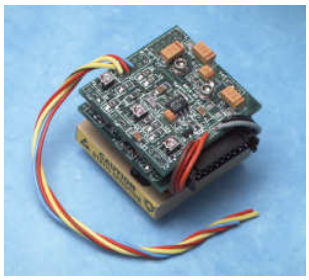
MICRO LAMBDA WIRELESS, INC.

YIG DEVICE (RD SERIES) DRIVERS
DIGITAL REMOTE SERIES
FOR ELECTROMAGNETIC DEVICES
.5-50 GHz

FEATURES

- All Electromagnetic Oscillators and Filters
- Compensation for Temperature Drift
- Voltage Regulators for Improved Stability
- 12 Bit Tuning Resolution
- Remote Device/Driver Location



DESCRIPTION

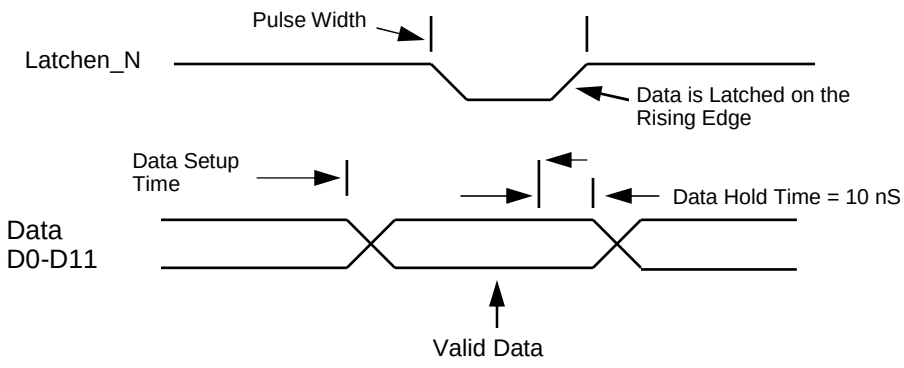
All Micro Lambda Electromagnetic YIG Devices are available with remotely located digital driver circuits. These drivers eliminate the need for customers to design or develop their own circuits and sophisticated test and alignment procedures. These remote drivers can be aligned at Micro Lambda's factory to ensure peak performance. Alignment and compensation with the particular YIG Device can be maximized down to the component level.

All drivers in this series provide input voltage regulators and compensation circuits to improve frequency drift. All voltages required by the YIG Device, except the heater inputs are supplied by the voltage regulators.

COMMERCIAL DIGITAL DRIVERS	.5-50 GHz YIG DEVICE, DIGITAL SERIES
DRIVER INPUT & RESPONSE	SPECIFICATION (0 to + 65 deg. C)
Tuning Command	Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency
Tuning Resolution	12 BIT Positive Logic (Fmax-Fmin)/4095 Resolution All Data Bits have Internal 10k ohm Pull-up Resistor to +5V
Frequency Accuracy (Note 1) (excluding hysteresis)	YIG Device Accuracy +2 MHz
Tuning Speed	5 mSec for 1 GHz step to within +/-10 MHz.
Main Driver Inputs	
Supply Voltage & Current (Note 2)	
+15 V +/- .5 V	YIG Device Tuning Current + 100 mA, Max.
-15 V +/- .5 V	100 mA, (Plus Oscillator –5 Vdc Current if any) Max.
Supply Voltage Pushing	+/- .2%MHz Max. @ .5Vdc (2-3000 kHz)
Supply Voltage Ripple	10 mV Ripple Pk-Pk from 2 kHz to 3 MHz
Ground	Chassis Ground
YIG Heater Voltage & Current (Note 3)	750 mA surge for 2 seconds, 150 mA steady state
+24 Vdc ±4 Vdc	Polarity independent : ±12 Vdc or ±15 Vdc acceptable
Latch Enable	LATCHEN_N is a TTL, 5V CMOS control line. It has an internal 10k-ohm pull-up resistor to +5 V. It is used to transfer the data on the bus to the digital driver circuit. TTL high = data ignored. Connect to Ground if enable is not required. If the unit is to be used on a computer data bus, the timing Diagram below applies. (All times = Minimum) 10 nS rise/fall latch transitions.

Note 1: Accuracy Includes Temperature Drift & Linearity.
2. Some YIG devices require higher voltages - Check with factory.
3. See particular YIG Device specification for heater current requirements.

TIMING DIAGRAM



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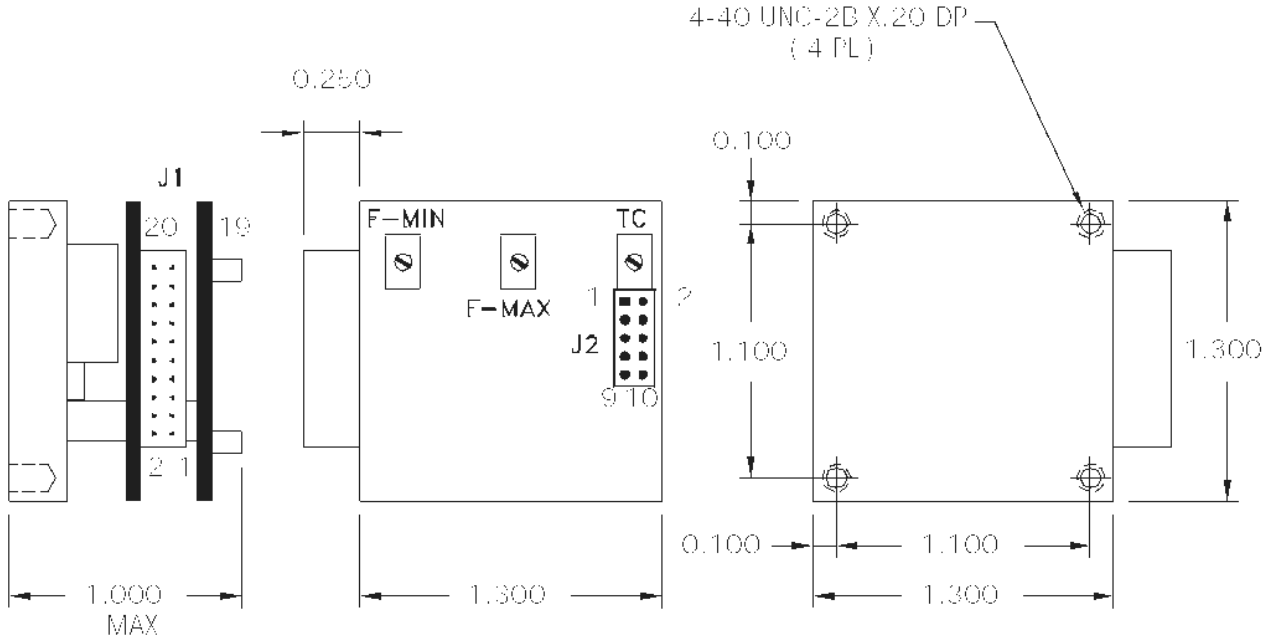

WEIGHT: 6 Oz

BOTTOM BOARD (DAC BOARD)
J1–INPUT (2MM DUAL ROW TERMINAL STRIP)

DIGIKEY PART # : H2069-ND
MATING WITH # : H2027 ND OR H2036 ND
CRIMP CONTACT : H2139 ND

PIN	*FUNCTIONS*	*PIN*	*FUNCTIONS*	
1	DATA BIT 0(LSB)	11	DATA BIT 10	
2	DATA BIT 1	12	DATA BIT 11(MSB)	
3	DATA BIT 2	13	LATCHEN N	
4	DATA BIT 3	14	GND	
5	DATA BIT 4	15	SUPPLY +(15V)	
6	DATA BIT 5	16	SUPPLY -(15V)	
7	DATA BIT 6	17	HEATER +	
8	DATA BIT 7	18	HEATER	
9	DATA BIT 8	19	FM –	(*)
10	DATA BIT 9	20	FM -	(*)

TOP BOARD (DRIVER BOARD)
J2–OUTPUT CONNECTION TO YIG

PIN	*FUNCTIONS*	
1	TUNE COIL	
2	TUNE COIL	
3	FM +	(*)
4	FM -	(*)
5	OSC. VCC(+15V)	(*)
6	-5V	(*)
7	HEATER	
8	HEATER	
9	GND	(*)
10	-5V (OPTIONAL)	(*)

NOTES:
1 ( ) : NOT USED FOR FILTER
2- RECOMMENDED WIRE SIZE – 22-24 A.W.G

	MICRO LAMBDA, INC.			
	1.3" DIGITAL DRIVER (1.3 X 1.3 X 1.0")			
	SIZE	51 002		C